Nitisman Mishra

Email: nitishmanmishra@gmail.com **Mobile**: 8638578478/8876305725

WORK EXPERIENCE

Assistant Professor, Department of Electrical Engineering, Assam Engineering College *Feb 2025 - Present*

Intel Corp. Bangalore– SoC Design Engineer *Aug 2021 - Feb 2025*

- Worked on GNRD project- I was in the timing team. I closed timing of fuse partition. I wrote scripts to automate DRC/signoff checks. I wrote scripts for checking slope/crosstalk/duty cycle distortion on critical ERROR signal paths.
- Worked on IMHD project- I was the Timing owner of a tile. I provided guidance on timing/clock tree synthesis.
- Worked on IMH1 project- I was responsible for handling PT-ECO flow and signoff/DRC checks of 3 tiles. I generated automated/manual timing ECOs and provided guidance on fixing Cap/Slope related violations.

Cirel Systems, Bangalore – Analog Design Engineer Intern *May 2020 – July 2020*

- I worked on developing a voltage reference in CMOS considering slow/fast/nominal corners; and temperature range -40 to 125 degree Celsius. The circuit started off as a 2 transistor design which later incorporated feedback to exhibit low temperature coefficient of voltage characteristics.

EDUCATION

Indian Institute of Science, Bangalore *2019 - 2021*

M.Tech. Electrical Engineering – 1st class with Distinction

- I worked on the development of an interface relay for micro grid protection using Nexys4DDR FPGA. I wrote the VHDL code for Phase locked loop, Island detection logic, Synchronization logic, Overcurrent protection logic, interfacing DAC/ADC with FPGA. The simulations were done in Simulink. The circuit implementation was done using VHDL in Xilinx Vivado. The testing of the relay was done using signals generated from National Instruments CDAQ system/LabView.

Assam Engineering College, Guwahati *2015 - 2019*

B.E. Electrical Engineering - 1st class with Honors

Kendriya Vidyalaya, Barpeta *2003 - 2015*

AISSE 10.0 CGPA, AISSCE 92%

SKILLS/TOOLS

- Static Timing Analysis- Synopsys Primetime, Synopsys PT-ECO
- Analog Simulations- Cadence Virtuoso, KiCad/LTSpice
- VHDL based FPGA design- Xilinx Vivado
- Scripting- Linux, TCL/TK
- Programming- C, Python

ACHIEVEMENTS

- GATE EE 2019 - Rank 339, Score 827
- CBSE Problem Solving Assessment 2013-14- Percentile scores of 96.43, 99.73, 95.96 in Language conventions, Qualitative Reasoning, Quantitative Reasoning respectively